AMENDMENTS TO THE CLAIMS:

1-10. (cancelled)

11. An image generation circuit, comprising:

a preprocessing portion operably coupled to receive primitive parameters, wherein the preprocessing portion produces pixel information from the primitive parameters based on the primitive parameters;

a pixel engine operably coupled to the preprocessing portion, wherein the pixel engine receives the pixel information, and calculates intermediate data from the pixel information; and

a memory operably coupled to the pixel engine, wherein the memory stores the intermediate data,

wherein the pixel engine reads the intermediate data from the memory and calculates a final data from the fed-back intermediate data.

12. A image processing circuit, comprising:

a preprocessing block that receives primitive parameters and produces pixel information from the primitive parameters;

a pixel engine operably coupled to the preprocessing block, wherein the pixel engine generates pixel values from the pixel information; and

a feedback path from an output portion of the pixel engine to an input portion of the pixel engine, wherein the feedback path allows results of operations performed by the pixel engine to be used in subsequent operations performed by the pixel engine.

13. The image processing circuit of claim 12, wherein the feedback path includes buffering such that a plurality of pixels can be processed during each of a plurality of passes in a multipass operation, wherein each pass has associated information that is used to configure the image processing circuit.